In the Specification

Please amend the title as follows:

Methods of Forming Semiconductor Circuitry~~, and Semiconductor Constructions~~.

At page 1, before the "Technical Field" section, please insert the following paragraph:

RELATED PATENT DATA

This patent resulted from a divisional application of U.S. Patent Application Serial No. 09/989,931, which was filed on November 21, 2001.

Please amend paragraph [0040] on pages 12-13 as follows:

[0040] Fig. 8 is a top view of semiconductor construction 10, and diagrammatically illustrates a zonal configuration of one embodiment of the present invention. The construction of Fig. 8 is shown at a processing step corresponding to that of Fig. 6. Semiconductive material mass 30 extends around an exposed portion ~~50~~ 51 of monocrystalline material 16. In other words, upper surface 32 of mass 30 encircles the exposed portion ~~50~~ 51 of monocrystalline mass 16. Another exposed portion ~~52~~ 53 of mass 16 is shown outwardly of mass 30 relative to the encircled exposed portion ~~50~~ 51. The first semiconductor circuit component 36 of Fig. 7 can correspond to a portion of a DRAM array, and such DRAM array can be formed in the encircled exposed portion ~~50~~ 51 of monocrystalline mass 16. The second semiconductor circuit component 38 can correspond to a portion of circuitry formed peripheral to the DRAM array, and in the shown embodiment can correspond to a portion of circuitry which encircles the DRAM array. The

memory array can be entirely over the exposed portion of monocrystalline material 16, and accordingly not over mass 30. In other words, the invention encompasses embodiments wherein no DRAM cells are formed over mass 30, but instead an entirety of the DRAM cells of an integrated circuit construction are over the exposed monocrystalline material 16.